In-Rush Current Limit MOSFET Driver

Features

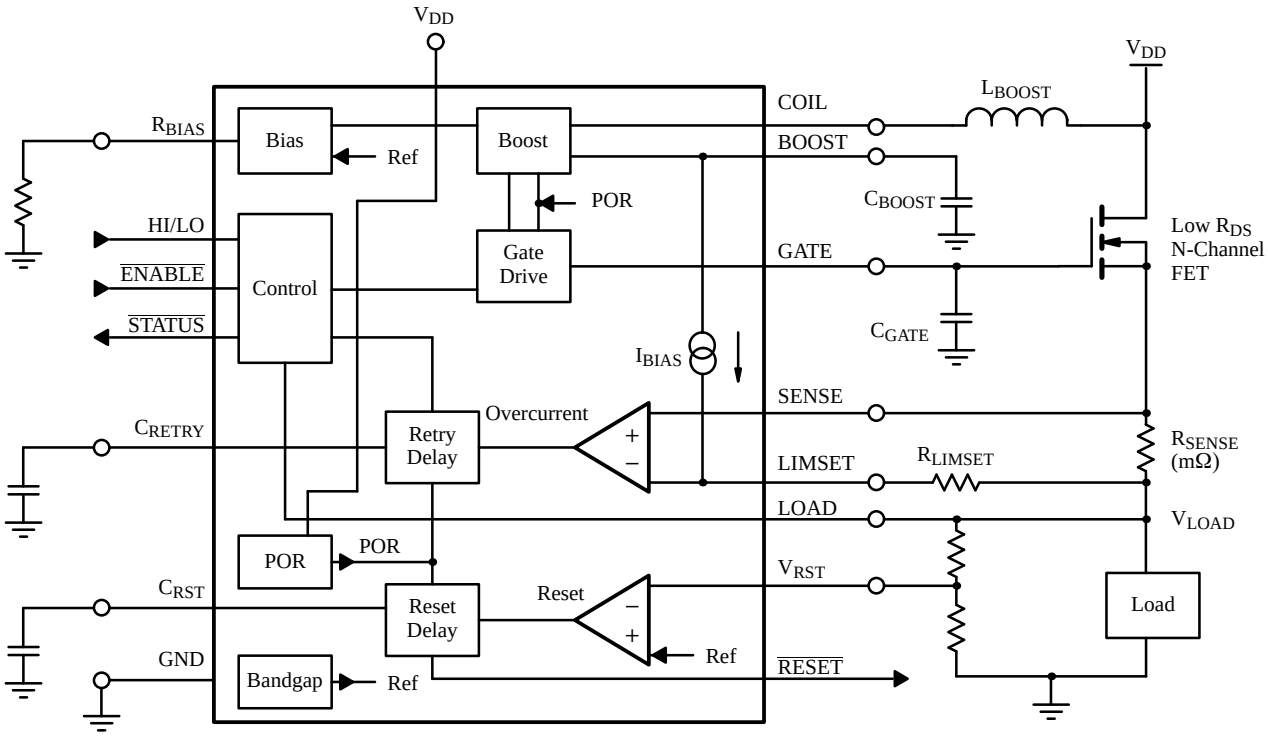
- 2.9- to 13-V Input Operating Range
- Microprocessor $\overline{\text{RESET}}$
- Integrated High-Side Driver for N-Channel MOSFET
- Programmable di/dt Current

Description

The Si9750 current limit MOSFET interface IC is designed to operate between a power source and a load using a low on-resistance power MOSFET with a sense terminal or in conjunction with a low ohmic sense resistor. The Si9750 current limiter prevents source and load transients during hot swap and power-on with programmable dv/dt and di/dt. Both turn-on and steady-state current limits can be individually programmed, providing protection against short circuits. Power on $\overline{\text{RESET}}$ and logic controls allow complete microprocessor interfacing. The $\overline{\text{RESET}}$ function of the Si9750 is industry-standard with full programmability.

The Si9750 is available in a 16-pin SOIC package and is rated over the commercial temperature range (0 to 70°C).

Functional Block Diagram



Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1332 .

Absolute Maximum Ratings

Voltages Referenced to Ground
V_{DD} . . . . . 15 V
Boost Voltage . . . . . 29 V
Inputs/Outputs
(except Gate, Boost and V_{RST}) . . . . . –0.3 to V_{DD} + 0.3 V
V_{RST} Input Current (0 < V_{RST} < 15 V) . . . . . 20 mA
Inputs/Outputs Current . . . . . 20 mA
$\overline{\text{RESET}}$ Current . . . . . 3 mA
$\overline{\text{STATUS}}$ Current . . . . . 3 mA

Storage Temperature . . . . . –65 to 125°C
Junction Temperature . . . . . 150°C
Power Dissipation (package)[a]
16-Pin SOIC[b] . . . . . 900 mW
Thermal Impedance (Θ_{JA}) . . . . . 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time*

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.9 V ≤ V_{DD} ≤ 13.2 V HI/LO = GND, R_{BIAS} = 12.5 kΩ L_{BOOST} = 100 µH, C_{BOOST} = 100 nF	Limits 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Supply						
Quiescent Current	I_Q	$\overline{\text{ENABLE}}$ =Logic Low		4	8	mA
Logic						
Enable Turn-On Voltage	$V_{EN(on)}$				0.3 x V_{DD}	V
Enable Turn-Off Voltage	$V_{EN(off)}$		0.7 x V_{DD}			
Enable Source Current	I_{ENSRC}	V_{ENABLE} = 0V	40		120	µA
Turn-On Time	t_{ON}	See Figure 3.			5	µs
Turn-Off Time	t_{OFF}				5	
Turn-On Boost	$t_{ON(BST)}$	See Figure 4.			600	
t_{OFF} Initial Short Circuit	$t_{OFF(ISC)}$	C_{GATE} = 33 nF, See Figure 6.			10	
t_{OFF} Short Circuit	$t_{OFF(SC)}$	C_{GATE} = 33 nF, See Figure 7.			2	
Status Output Voltage	V_{STAT}	I_{SINK} = 200 µA			0.4	V
Status Output Delay Time	t_{STDLY}	See Figure 8.			25	µs
Status Threshold	$V_{STATTHR}$		0.85 x V_{DD}		0.95 x V_{DD}	V
HI/LO Turn-On Voltage	$V_{HILO(on)}$		0.7 x V_{DD}			
HI/LO Turn-Off Voltage	$V_{HILO(off)}$				0.3 x V_{DD}	
Gate Drive						
Enhancement Voltage (V_{GATE} – V_{SENSE})	V_{GS}		8.5	10.5	15	V
Source Current	I_{SOURCE}	V_{CBOOST} = 9 V	1.06	1.30	1.54	mA
Sink Current	I_{SINK}		1.6	2.6	3.7	

Specifications

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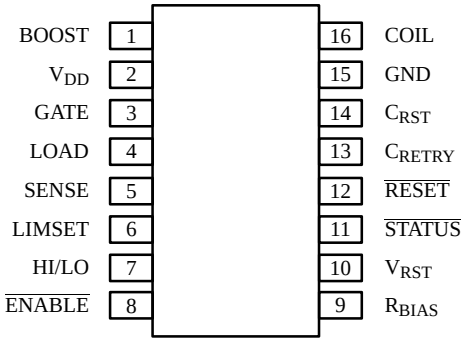
Current Sense Circuit						
Current Sense Amplifier Common Mode Range	V_{CMR}		0		V_{DD} + 0.3	V
Current Sense Amplifier Voltage Offset	V_{OS}		–3		3	mV
Current Sense Amplifier Bias Current	I_{SOS}	Normal Operation		–0.2		µA
R_{LIMSET} Reference Current	$I_{RLIMSET}$		18	19.5	21	
Current Sense Amplifier Hysteresis	V_{HYST}			12		mV
Current Sense Amplifier Series Offset	V_{SOS}	HI/LO = V_{DD}, V_{CMR} > 0.5 V		20		
Power On Reset						
$\overline{\text{RESET}}$ Output Voltage	$V_{OP(rst)}$	I_{OUT} = 1 mA, V_{DD} > 2 V			0.4	V
$\overline{\text{RESET}}$ Output Hysteresis[c]	V_{HYST}	See Note c		2		mV
$\overline{\text{RESET}}$ Comparator Input Threshold	V_{RST}		1.223	1.250	1.277	V
$\overline{\text{RESET}}$ Comparator Offset Voltage[d]	V_{RBIAS}			0.5		mV
$\overline{\text{RESET}}$ Comparator Input Bias Current	I_{BIAS}			–0.2		µA
$\overline{\text{RESET}}$ Timer Delay	t_{RSTD}	C_{RST} = 15 nF, See Figure 8.	110	150	190	µs
RETRY	t_{RETRY}	C_{RETRY} = 100 nF	70	130	200	ms

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production test.
c. In a practical situation, V_{HYST} is multiplied by ratio of a resistor divider chain. For V_{DD} = 13.2 V, V_{HYST} = 20 mV.
d. The $\overline{\text{RESET}}$ comparator input threshold specification (V_{RST}) includes the $\overline{\text{RESET}}$ comparator offset voltage.

Pin Configuration

SO-16



Top View

Order Number: Si9750CY

Pin Description

Pin Number	Function	Description
1	BOOST	Output of on-chip Boost converter. A 100-nF capacitor should be connected between BOOST and GND
2	V_{DD}	Positive supply pin.
3	GATE	Connection to external power MOSFET gate.
4	LOAD	Connection to positive supply side of LOAD.
5	SENSE	Connects external sense resistor of a sensefet sense pin to SENSE input of overcurrent trip comparator. A standard MOSFET may also be used in conjunction with a low ohmic value shunt resistor.
6	LIMSET	Connects overcurrent limit set resistor R_{LIMSET} to the reference input of overcurrent trip comparator.
7	HI/LO	CMOS logic input to control the overcurrent trip comparator sensitivity at power-on. HI/LO should be connected to GND for low Capacitive loads and to V_{DD} for high capacitive loads.
8	$\overline{ENABLE}$	CMOS logic input to turn IC on or off. GATE voltage remains low when $\overline{ENABLE}$ is high.
9	R_{BIAS}	A resistor connected from this pin to GND programs the reference bias current for the overcurrent trip comparator resistor R_{LIMSET} and the $GATE_{(on)}$ charge current. See Functional Description for equations.
10	V_{RST}	Input to voltage monitor comparator.
11	$\overline{STATUS}$	Open drain NMOS output. This pin is driven low when the current limiter is enabled and the LOAD voltage is greater than 90% of V_{DD}.
12	$\overline{RESET}$	Open drain NMOS output. This pin is driven low during power on reset or when V_{RST} is lower than the internal 1.25-V reference.
13	C_{RETRY}	A capacitor connected from this pin to GND programs the retry timer.
14	C_{RST}	A capacitor connected from this pin to GND programs the reset timer.
15	GND	Negative supply pin.
16	COIL	Connection to Boost converter inductor.

Functional Description

The Si9750 together with an n-channel MOSFET provides the following functions:

- limits di/dt current for hot insertion applications
- provides complete short circuit protection
- high-side drive allows n-channel MOSFET to be used, for lower power dissipation
- industry-standard microprocessor reset function
- logic control input and outputs

Setting the Current Limit (SENSE, HI/LO pins, R_{LIMSET}, R_{SENSE})

The current limit point is determined by the voltage across R_{SENSE}, the value of R_{LIMSET}, and the bias current. The current limit circuit is shown in Figure 1.

The steady state current is set by the equation:

$$I_{LOAD} \times R_{SENSE} > I_{BIAS} \times R_{LIMSET} \quad \textbf{(1)}$$

Due to the highly capacitive nature of some loads, the Si9750 has an option to increase the current limit point to a much higher level at turn-on. In this case, turn-on is defined as $V_{GATE} < V_{DD} + 7.8$ V. This function is implemented with the HI/LO pin. If the HI/LO pin is tied low the current limit is 20% higher during turn-on than the steady state current limit point.

$$I_{LOAD} \times R_{SENSE} > 1.2 \times I_{BIAS} \times R_{LIMSET} \quad \textbf{(2)}$$
(with pin HI/LO=Low)

If a higher current limit is needed at start-up, the HI/LO pin can be tied high. The equation becomes:

$$I_{LOAD} \times R_{SENSE} > 1.2 \times I_{BIAS} \times R_{LIMSET} + I_{BIAS}(1\ k\Omega + R_{HI}) \quad \textbf{(3)}$$
(HI/LO = High)

Notice that any current limit can be set at turn-on using an optional resistor, R_{HI}.

Relaxation Mode Current Limit (C_{RETRY} pin)

In an overload condition, the Si9750 will go into a relaxation mode current limit operation that not only protects the source and load, but also reduces the power dissipated in the MOSFET. When an overload is detected, the circuit quickly turns off, then goes into a retry mode whereby the current is ramped up slowly. If the fault still exists, the current will ramp down again. This sequence will repeat indefinitely at a period defined by $10^6 \times C_{RETRY}$ until the fault is removed. Typically, capacitors in the range of 1 nF to 1 µF can be used on C_{RETRY}, but the period should be >50 ms.

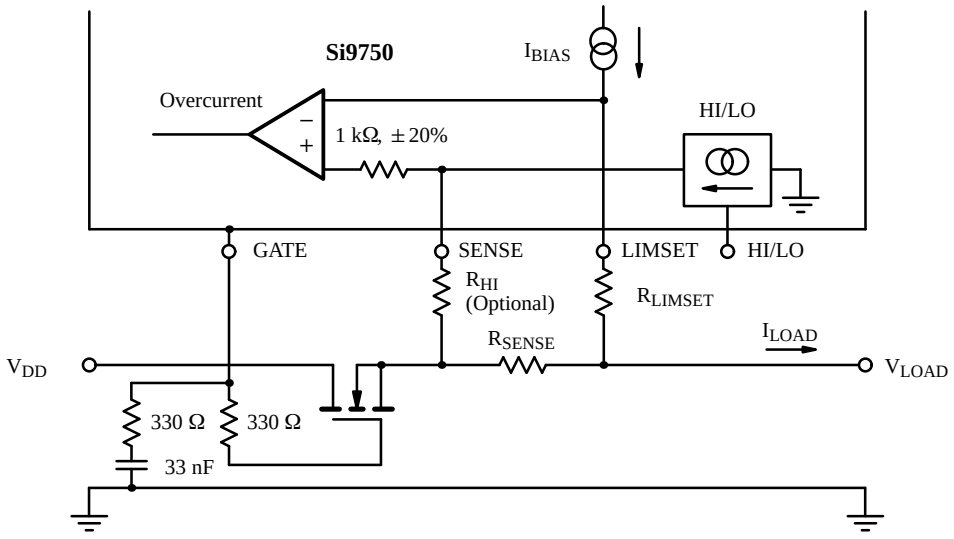


Figure 1.

Functional Description (Cont'd)

di/dt Limiting On Hot and Cold Insertion (GATE pin)

The GATE pin provides a constant current source that is used to control the rate of rise of the gate of the MOSFET, and hence to control the di/dt of the load and source current. The equation that governs the gate current is:

$$I_{SOURCE} = 1.25\ V \times \frac{12}{R_{BIAS}} = 1.2\ mA \quad \text{(for } R_{BIAS} = 12.5\ k\Omega\text{)} \qquad \textbf{(4)}$$

Typically, a 33-nF capacitor should be connected from the GATE pin to ground. If a large I_{SOURCE} is needed for high di/dt, a 330-Ω resistor in series with C_{GATE} may be necessary to prevent oscillation. In the case that V_{DD} > 6 V, a resistor of approximately 330 Ω is also recommended in series with the gate. (Figure 1.)

Reference Bias Current (R_{BIAS} pin)

This pin sets the internal current used by R_{LIMSET} to determine all the current limit points. Typically R_{BIAS} = 12.5 kΩ which sets a 20-µA bias current. The equation which relates R_{BIAS} to I_{BIAS} is:

$$I_{BIAS} = \frac{1.25\ V}{5 \times R_{BIAS}} = 20\ \mu A \quad \text{(for } R_{BIAS} = 12.5\ k\Omega\text{)} \qquad \textbf{(5)}$$

Power on Reset (POR) (V_{DD} pin)

This function monitors the voltage on the V_{DD} pin and signals the system if all input voltage requirements have been met. At turn-on when V_{DD} > 2.7 V ± 200 mV, a POR signal is generated for a duration of 100 µs. After this point the system is released into operation. If V_{DD} falls below 2.7 V ± 200 mV, a second POR signal will be generated. If two POR signals are detected, this indicates that the source for V_{DD} is not capable of supplying the load current. The IC then turns off the MOSFET and initiates its retry period, hence fully protecting the MOSFET from an over-power condition.

Boost Converter (COIL, BOOST pins)

The boost converter generates the gate drive for the external n-channel MOSFET. This is limited to typically V_{DD} + 11 V. The boost inductor should typically be 100 µH, <3.5 Ω, >180 mA dc, and the boost capacitor should be 100 nF.

Logic Control ($\overline{STATUS}$, $\overline{ENABLE}$, $\overline{RESET}$, V_{RST} and C_{RST} pins)

$\overline{STATUS}$. The status monitor detects when the load voltage is 90% of input voltage, $V_{LOAD} > 0.9 \times V_{DD}$. This pin is an open-drain NMOS output, capable of sinking 200 µA at V_{OL} = 0.4 V. If this pin is used in conjunction with the $\overline{ENABLE}$ of another unit, power supply sequencing (or daisy-chaining) is easily implemented.

$\overline{ENABLE}$. This CMOS logic compatible input serves as the on/off control pin. This pin has 40-µA minimum pull-up to V_{DD}.

$\overline{RESET}$ (V_{RST}, C_{RST}, $\overline{RESET}$ pins). This is a standard implementation of the microprocessor reset function. A comparator looks at the voltage on V_{RST} pin and compares it with 1.25 V. This function is programmable by using an external voltage divider. When V_{RST} is higher than 1.25 V, the reset signal is delayed by the C_{RST} pin, defined by Equation (6) and then goes high. (Figure 8.)

$$\text{Reset delay } t_{RSTD} \approx 10^4 \times C_{RST} \qquad \textbf{(6)}$$

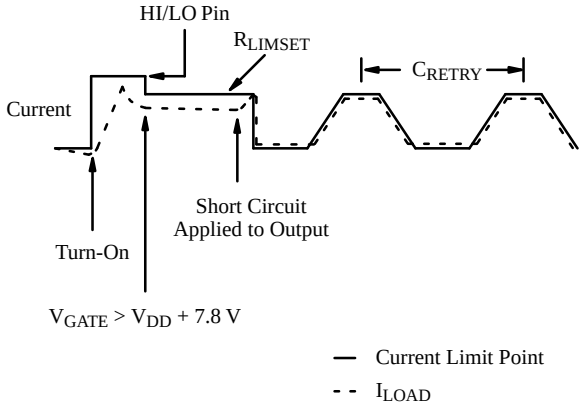
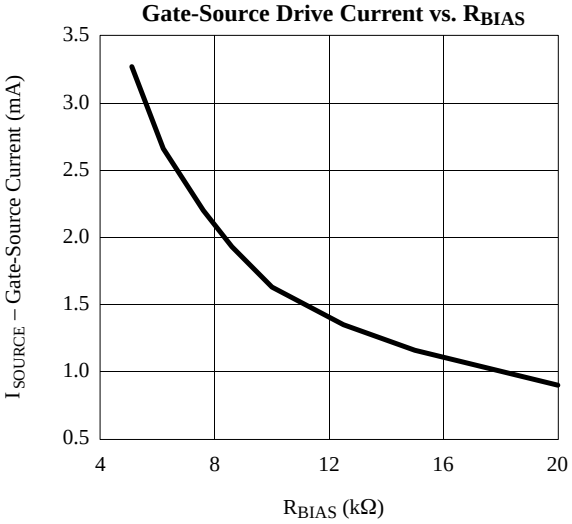


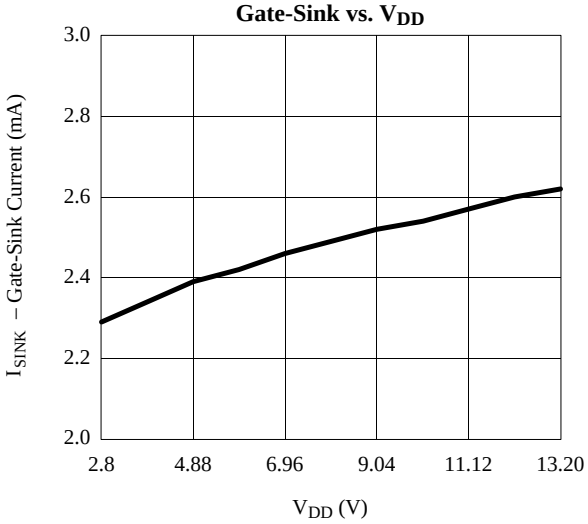
Figure 2. Typical Operation Under Start-up Condition With An Overcurrent Fault Applied to the Output

Typical Characteristics (25°C Unless Noted)

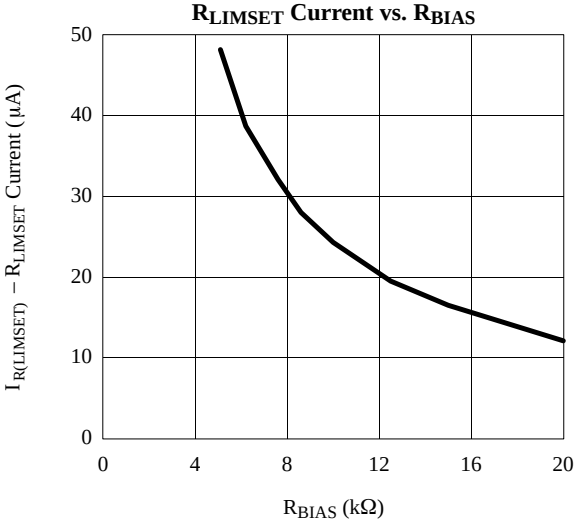
Gate-Source Drive Current vs. R_{BIAS}



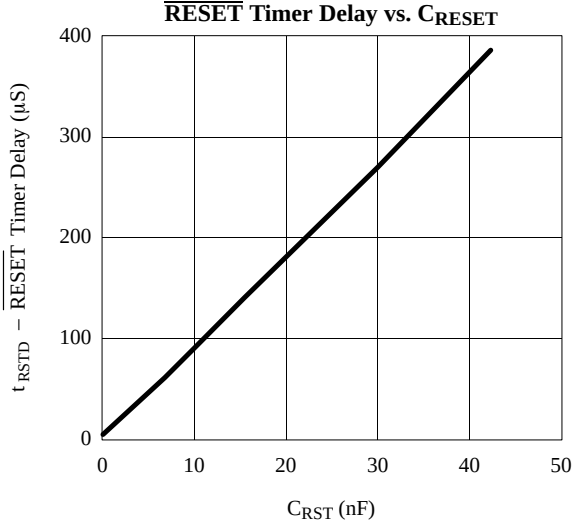
Gate-Sink vs. V_{DD}



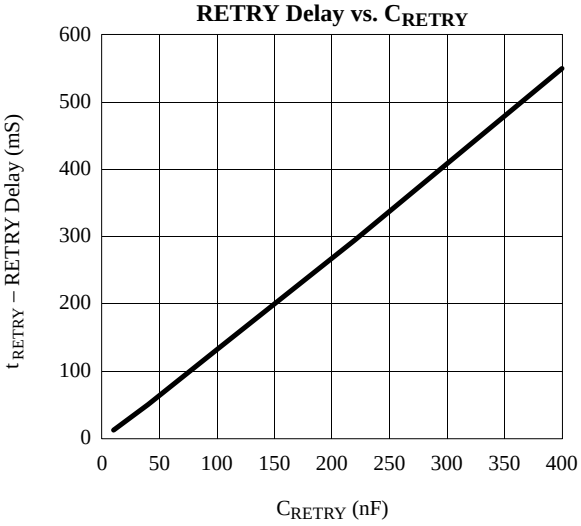
R_{LIMSET} Current vs. R_{BIAS}



$\overline{\text{RESET}}$ Timer Delay vs. C_{RESET}



RETRY Delay vs. C_{RETRY}



Switching Time Test Circuits

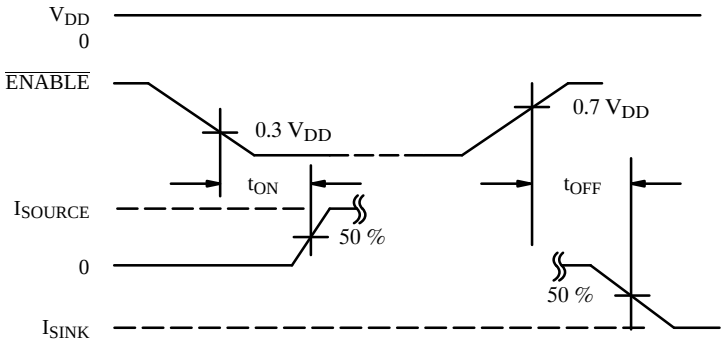


Figure 3. Normal-Mode Operation

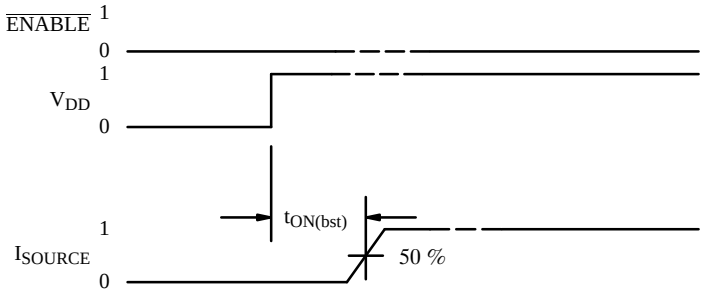


Figure 4. Timing Definition with $\overline{\text{ENABLE}}$ Already On

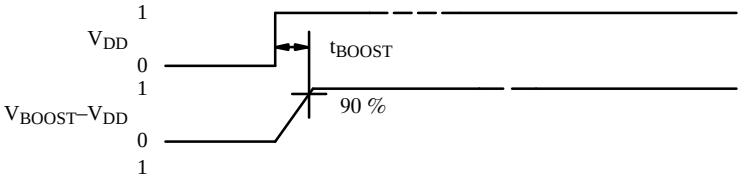


Figure 5. Start of Boost Converter

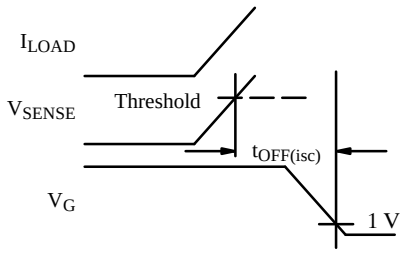


Figure 6. First Short Circuit

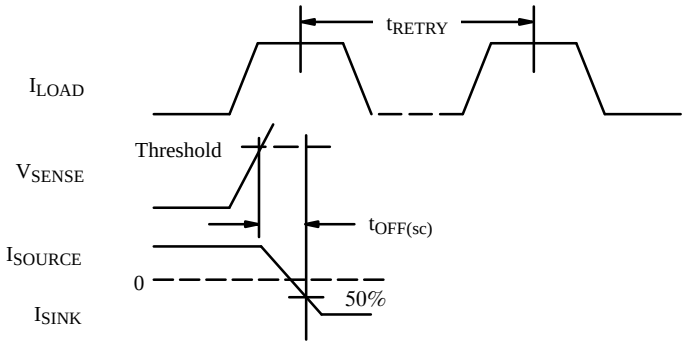
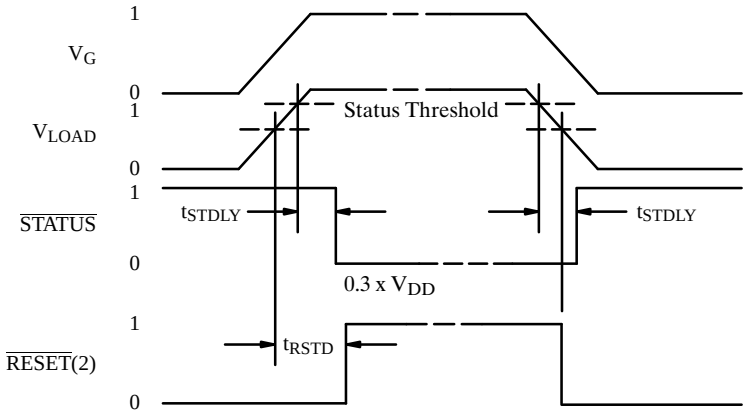


Figure 7. Relaxation-Mode Current Limit

Switching Time Test Circuits



(2) With reset input divider correctly set, monitoring V_{LOAD}

Figure 8. $\overline{STATUS}$ and $\overline{RESET}$